Claim Rejections Under 35 USC §112

Claim 2 is rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Claim 2 has been amended to alleviate the Examiner's rejections. A reconsideration for allowance of claim 2 is respectfully requested of the Examiner.

Claim Rejections Under 35 USC §102

Claims 26-33 are rejected under 35 USC §102(e) as being anticipated by Mclnick et al '899. It is contended that Mclnick et al discloses an electronic structure including electrically resistive via 120, and furthermore, the via is formed of a material having a resistivity of at least 100 Ω-cm.

The rejection of claims 26-33 under 35 USC §102(e) based on Mclnick et al is respectfully traversed.

Mclnick et al discloses a capacitor electrode having conductive regions adjacent a dielectric post. Figure 18 of Mclnick et al best describes the invention as shown in col. 8, lines 24-28 and lines 53-56:

> "Figure 18 further illustrates a cross-section of the embodiment previously illustrated in Figure 5 and further includes elements that form a capacitor. Overlying the adhesion/ barrier layer 122 and the electrode 50, illustrated in Figure 18, is a capacitor dielectric film 1801. ... The combination of the transistor 118, **oxygen barrier material** 120, and conductive fill material 116 (the storage node), and the capacitor 1804 forms a typical dynamic random access memory (DRAM)bit cell."

The Applicants respectfully submit that 120 shown by Mclnick et al is an oxygen barrier material, and therefore, not an electrically resistive via, as contended by the Examiner. Furthermore, Figure 18 shows a typical DRAM bit cell which is a combination of a transistor 118 and a capacitor 1804. There is no resistor in a typical DRAM bit cell, nor is it shown in Figure 18.

Furthermore, independent claim 26 recites:

"Claim 26. An electronic structure having an in-situ formed unit resistor in electrical communication with a capacitor comprising:

a unit resistor formed by a first conductive element and a second conductive element situated in different levels in said electronic structure connected therein-between by an **electrically resistive via**, said electrically resistive via being formed of **a material having a resistivity of at least 100 Ω-cm**; and

a capacitor formed juxtaposed to and in electrical communication with said unit resistor."

The Applicants respectfully submit that Mclnick et al does not show an electrically resistive via, let alone a via formed of a material having a resistivity of at least 100 Ω-cm.

The rejection of claims 26-33 under 35 USC §102(e) based on Mclnick et al is respectfully traversed. A reconsideration for allowance of these claims is respectfully requested of the Examiner.

Based on the foregoing, the Applicants respectfully submit that all of the pending claims, i.e. claims 2 and 26-33, are now in condition for allowance. Such favorable action, together with the passage to issuance of the allowed claims 1 and 3-14, is respectfully solicited.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "Version With Markings To Show Changes Made".

In the event that the present invention is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In The Specification

Paragraph beginning at line 5 of page 21 through page 22, line 10, has been amended as follows:

Figure 2A illustrates an enlarged, cross-sectional view of a present invention structure 10 similar to that of Figure 1G, but on an insulating [substrate] layer 12. A plane view of the electronic structure 10 is shown in Figure 2B. The versatility of the present invention process for forming electronic structures with in-situ formed unit resistors 24 is thus shown in Figures 2A and 2B. For instance, to form a unit resistor that has a single resistance value of 1R, the structure shown on the left side of Figure 2B can be utilized which includes a conductive element 28 with node D1 electrically connected to a single electrically resistive via 24 and a conductive element 16 with a node D2. The circuit shown on the right side of Figure 2B indicates that a resistance value of 2R can be obtained between the conductive element 30 with anode D3 and the conductive element 42 by flowing an electrical current through via 34 to metal 32, and from metal 32 via 36 to metal 42 which has two resistive vias connected in-

series. Via 34 and via 36 are connected in-series by conductive element 44. The resistance value obtained between the conductive element 30 and the conductive element 42 or to node D5 therefore doubles that obtained between the conductive element 28 and the conductive element 16. Similarly, by connecting via 36 and via 38 in-series by the conductive element 42, and then connecting via 38 to metal 48 or node D6 to have an electrical resistance of 3R. Furthermore, metal 30 or from node D3 through vias 34,36,38 and 40 in-series by the conductive element 46, or node D7, an electrical resistance of 4R may be obtained between the conductive element 30 and the conductive element 46. A versatile electrically resistive via network can thus be obtained for any suitable value of electrical resistance by utilizing the present invention novel method.

In The Claims

Claim 2 has been amended as follows:

2. (Amended) An electronic structure having in-situ formed unit resistors according to claim 1, wherein said pre-processed substrate is a semiconductor wafer [having a first dielectric material layer on top].

LTDR

SYMBOLS FOR DRAFTSMEN

Rule 84 (g) states that graphical symbols for conventional elements may be used on the drawing when appropriate, subject to approval by the Office. The symbols and other conventional devices which follow have been and are approved for such use. This collection does not purport to be exhaustive, other standard and commonly used symbols will also be acceptable provided they are clearly understood, are adequately identified in the specification as filed, and do not create confusion with other symbols used in patent drawings.

NOTES: In general, in lieu of a symbol, a conventional element, combination or circuit may be shown by an appropriately labeled rectangle, square, or circle; abbreviations should not be used unless their meaning is evident and not confusing with the abbreviations used in the suggested symbols. In the electrical symbols an arrow through an element indicates variability thereof, see for example symbols 2, 6, 12; dotted line connection of arrows indicates ganging thereof, see symbol 6; inherent property (as resistance) may be indicated by showing symbol (for resistor) in dotted lines.